REMARKS

Applicants amend claim 8 to more appropriately define the claimed subject matter. Claims 2, 4, and 8-11 are pending in this application.

103(a) Rejection of Claims 2, 4, and 8-11 over *Ooishi* in view of *Branch et al.*

The Examiner rejected claims 2, 4, and 8-11 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,271,710 to Ooishi ("*Ooishi*") in view of U.S. Patent Application Publication No. 2003/0076179 to Branch et al. ("*Branch et al.*"). Applicants respectfully traverse the rejection because a prima facie case of obviousness has not been established.

There are three criteria required to establish a prima facie case of obviousness. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). M.P.E.P. § 2142, 8th Ed., Rev. 2 (May 2004), p. 2100-128.

Claims 2, 4, and 8-11 are allowable over *Ooishi* in view of *Branch et al.* for at least the reason that *Ooishi* and *Branch et al.* fail to disclose each and every limitation recited in independent claim 8, from which claims 2, 4, and 9-11 depend. For example,

Ooishi and *Branch et al.* fail to disclose a "**circuit for providing a refresh cycle for a memory device**" comprising, inter alia, a "**frequency generator comprising (i) a capacitor having a terminal to receive the summed first and second currents and (ii) a comparator to compare a voltage at the terminal of the capacitor to a reference voltage and generate an output signal that indicates when the voltage at the terminal of the capacitor exceeds the reference voltage**," as recited in amended claim 8.

Ooishi fails to teach or suggest the "frequency generator" recited in claim 8. The Examiner relies on the "ring oscillator 30" (shown in Figure 3) of *Ooishi* as constituting a "frequency generator." The Examiner contends that "figure 4 shows all limitations of the claim except for the detail of the ring oscillator 30. However, Branch et al.'s figure 3a shows a ring oscillator having low Jitter. Therefore, it would have been obvious to one having ordinary skill in the art to us[e] Branch et al.'s ring oscillator for Ooshi's oscillator 30 for the purpose of saving power consumption. Thus, the modified Ooshi's figure 4 shows that the frequency generator comprises a comparator (figure 4) to compare two input signals (VIP, VIN) and generate an output signal (VOM) that indicate which of the two input is larger (VOM will be high if VIP is lower than VIN, and VOM will be low if VIP is higher and [*sic*] VIN) is and a capacitor (C1-C3)." (Office Action of 5/22/06, pg. 2, paragraph 4 to pg. 3, paragraph 1.)

The Examiner's rejection in the first paragraph at page 3 of the Office Action is unclear because neither of the figures cited by the Examiner, namely Figure 4 of *Ooishi* and Figure 3A of *Branch et al.*, shows input signals labeled VIP, VIN or an output signal labeled VOM. Since Figure 4 of *Branch et al.* is the only figure that Applicants can find

in either reference that shows input signals labeled V_{IP}, V_{IN} and an output signal labeled V_{OM}, it appears that the Examiner is relying on the circuit shown in this figure. As noted in *Branch et al.*, "[t]he fully symmetrical differential current steering delay cell used in the ring oscillators of 3a and 3b is displayed in more detail in FIG. 4" (paragraph [0034]).

However, not only does *Ooishi* fail to teach the frequency generator, but *Branch et al.* also does not make up for the deficiencies of *Ooishi* for at least the reason that *Branch et al.* also fails to teach or suggest "**a capacitor having a terminal to receive the summed first and second currents**," as recited in claim 8. Capacitors C1-C3 of *Branch et al.* relied on by the Examiner do not have "a terminal to receive the summed first and second currents," as required by claim 8. As shown in Figure 3A of *Branch et al.*, neither of the terminals of any of capacitors C1-C3 receives any "summed first and second currents." Thus, *Branch et al.* fails to teach or suggest "a capacitor having a terminal to receive the summed first and second currents," as recited in claim 8.

Additionally, *Branch et al.* does not make up for the deficiencies of *Ooishi* because *Branch et al.* also fails to teach or suggest "**a comparator to compare a voltage at the terminal of the capacitor to a reference voltage and generate an output signal that indicates when the voltage at the terminal of the capacitor exceeds the reference voltage**," as recited in claim 8. The "ring oscillator" of *Branch et al.* relied on by the Examiner does not comprise a "comparator," as recited in claim 8. Instead, Figure 3A of *Branch et al.* illustrates a ring oscillator that has three "differential inverting stages" (Figure 3A; pg. 2, paragraphs [0026] and [0028].) A differential inverting stage does not constitute a comparator. A comparator is a device that "compare[s] two analog input signals and generate[s] an output signal that indicates

which of the two analog input signals is larger," as required by claim 8. In contrast, a differential inverting stage is a "NOT" logic gate that inverts a digital signal at its differential inputs.

The Examiner apparently argues that the differential inverting stage inherently behaves as a comparator. However, a reference "is good only for that which it clearly and definitely discloses." *In re Hughes*, 345 F.2d 184, 188, 145 USPQ 467, 471 (CCPA 1965). Furthermore, "[a] claim limitation is inherent in the prior art if it is necessarily present in the prior art, not merely probably or possibly present." *Akamai Technologies, Inc. v. Cable & Wireless Internet Serv., Inc.*, 344 F.3d 1186, 1192, 68 USPQ2d 1186, 1190 (Fed. Cir. 2003). Based on what is clearly and definitely disclosed in *Branch et al.*, the differential inverting stage of *Branch et al.* does not inherently behave as a comparator for at least the reason that the output signal V_{OM} does not necessarily indicate which of the input signals (V_{IP}, V_{IN}) is larger.

Moreover, the differential inverting stage of *Branch et al.* does not "compare a voltage at the terminal of the capacitor to a reference voltage and generate an output signal that indicates when the voltage at the terminal of the capacitor exceeds the reference voltage," as required by claim 8. For example, the differential inverting stage of *Branch et al.* does not compare a voltage at a terminal of any of capacitors C1-C3 shown in Figure 3A to a reference voltage. Rather than being connected to one of the input terminals (V_{IP}, V_{IN}) of each differential inverting stage, "[c]apacitors, C_1, C_2, and C_3, are connected to the common mode current bias node, N1, N2, and N3, of each stage, respectively" (paragraph [0026]; emphasis added).

Furthermore, *Branch et al.* fails to teach or suggest that the voltages at the terminals of capacitors C1-C3 change such as to "exceed[] the reference voltage," as required by claim 8. Instead, "capacitors, C_1, C_2, and C_3 reduce the voltage variation on common mode nodes, N1, N2, and N3" (paragraph [0028]; emphasis added). Thus, *Branch et al.* fails to teach or suggest "a comparator to compare a voltage at the terminal of the capacitor to a reference voltage and generate an output signal that indicates when the voltage at the terminal of the capacitor exceeds the reference voltage," as recited in claim 8.

Thus, since *Ooishi* and *Branch et al.* fail to teach or suggest each and every element of claim 8, claim 8 and claims 2, 4, and 9-11 that depend therefrom are allowable over *Ooishi* in view of *Branch et al.* under 35 U.S.C. § 103(a).

CONCLUSION

In view of the foregoing amendments and remarks, Applicants respectfully request reconsideration and reexamination of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to Deposit Account No. 06-0916.

Respectfully submitted,

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Dated: August 18, 2006

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